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Efficient FPGA Implementation of CORDIC-Optimized Discrete Cosine Transform for Real-Time Image Compression

Jyoti Singh[1], Prof. Ashish Duvey[2]

[1,2]Department of Electronics and communication Shriram College of Engineering and Management, RGPV Bhopal, India

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ABSTRACT

The Discrete Cosine Transform (DCT) is widely used in image compression standards due to its energy compaction and decorrelation properties. However, its traditional multiplier-based implementation poses challenges in terms of hardware complexity, power consumption, and scalability on real-time embedded platforms. This paper proposes an efficient FPGA implementation of an 8-point DCT architecture optimized using the Coordinate Rotation Digital Computer (CORDIC) algorithm. By replacing multipliers with shift-add-based CORDIC units and minimizing rotation iterations through angle decomposition, the proposed architecture significantly reduces resource utilization. The design is developed in VHDL and synthesized using Xilinx ISE 14.1i on a Virtex-5 FPGA (XC5VFX100T). Simulation and synthesis results confirm functional accuracy, with a notable 19% reduction in 16-bit shift registers and adder-subtractor units compared to conventional DCT architectures. The output waveforms demonstrate precise frequency-domain transformation for various input sequences. The proposed approach is highly suitable for real-time image compression systems in power-constrained and resource-limited embedded applications.

Keywords: FPGA, Discrete Cosine Transform (DCT), CORDIC Algorithm, VHDL, Image Compression, Xilinx ISE, Hardware Optimization, Digital Signal Processing (DSP), Real-Time Processing, Low-Power Architecture.

INTRODUCTION

In today's digital era, the exponential growth of visual data has driven the demand for efficient and real-time image compression techniques. Whether in consumer electronics, medical imaging, satellite systems, or surveillance, the necessity for storing and transmitting large volumes of image data has intensified the research on compression algorithms and hardware-efficient implementations. Among various transformation techniques, the Discrete Cosine Transform (DCT) has remained the cornerstone of image and video compression standards due to its exceptional energy compaction and decorrelation properties [1], [2].

The 8-point DCT is particularly popular as it forms the computational core of international compression standards such as JPEG and MPEG. However, its traditional implementation, involving multiple floating-point multiplications, is computationally expensive and hardware-inefficient, making it unsuitable for resource-constrained and real-time embedded systems [3]. In response to these limitations, researchers have proposed various DCT approximations and optimized architectures to achieve faster and lower-power hardware implementations [4], [5].

One of the most promising approaches to reducing DCT complexity is the use of the Coordinate Rotation Digital Computer (CORDIC) algorithm, a shift-add algorithm that eliminates the need for multipliers and simplifies hardware implementation. CORDIC was originally developed for computing trigonometric functions, but its adaptability has extended its utility to transformations like DCT, DFT, and digital filters [6]. In particular, modified versions of CORDIC have been successfully used to approximate cosine values in DCT calculations, thereby reducing power consumption and resource utilization [7].

In recent years, various researchers have explored CORDIC-driven DCT approximations. Bayer et al. proposed low-power 16-point DCT approximations suitable for image compression and FPGA prototyping, demonstrating the benefits of replacing multipliers with CORDIC structures [4]. Similarly, Oliveira et al. introduced angle-based similarity methods to derive low-complexity 8-point DCT approximations that offered comparable performance to standard DCTs while reducing arithmetic operations [2]. Cintra and Bayer, in several influential works, proposed orthogonal and near-orthogonal DCT approximations that could be implemented using additions and bit-shifts alone [3], [9], [15].

Moreover, Kulasekera et al. [10] and Madanayake et al. [11] developed energy-efficient DCT approximations that significantly reduced power and area overhead on FPGA platforms. Their results revealed that the CORDIC-based architectures could be scaled and pipelined to match real-time constraints without degrading image quality. These insights were further validated by Dimitrov et al., who designed multiplier-less 8-point DCT blocks specifically optimized for video coding [13]. Beyond algorithmic simplifications, the importance of implementation platforms cannot be overstated. Field-Programmable Gate Arrays (FPGAs) have emerged as a viable solution for real-time image processing due to their inherent parallelism, reconfigurability, and low latency. VHDL-based designs mapped onto FPGAs like Xilinx Virtex and Spartan series have shown significant speedups in DCT computations compared to software solutions [5], [6], [8]. Edirisuriya et al. showed that FPGA prototypes of DCT approximations are not only feasible but also capable of achieving considerable savings in power and area compared to traditional DSP processors [16]. In line with this trend, the current study proposes an efficient hardware architecture for an 8-point DCT using optimized CORDIC processors, implemented using VHDL and synthesized on Xilinx ISE 14.1i targeting a Virtex-5 XC5VFX100T device. The novelty of this architecture lies in its ability to approximate cosine coefficients using minimum iterations of CORDIC rotation angles. For example, angles such as 7π/167\pi/167π/16 and 3π/163\pi/163π/16, traditionally computed using four or more iterations, are recalculated using just two or three iterations with minimal impact on output precision, thanks to careful selection of rotation indices iii based on the function tan−1(2−i)[17].

To further optimize the design, individual CORDIC modules are reused within the pipeline, and redundant adders/subtractors are eliminated using a modified butterfly-based structure. This leads to a 19% reduction in both 16-bit shift registers and arithmetic units compared to conventional DCT architectures, as also emphasized in comparative studies by Leite et al. [14] and Cintra et al. [17]. The simulation results using iSim confirm functional correctness, while synthesis results from Xilinx ISE reveal that the proposed design achieves operating frequencies in excess of 140 MHz, suitable for high-definition real-time image compression tasks. This aligns with findings from Bayer and colleagues [18], who showed similar performance improvements when implementing approximate transforms on hardware.

The proposed system is validated using several test input sequences, and the output waveforms demonstrate precise frequency-domain transformation of time-domain signals. Moreover, the resource utilization summary confirms the design's suitability for embedded applications where area, power, and throughput are critical constraints. This study contributes a scalable and power-efficient hardware solution for DCT computation, paving the way for real-time image compression in portable and embedded systems. By combining the mathematical elegance of the DCT with the hardware efficiency of CORDIC and FPGA platforms, the design serves as a promising alternative for future multimedia and signal processing applications. Furthermore, the methodology is extendable to larger DCT blocks (e.g., 16-point or 32-point), making it adaptable to evolving compression standards and resolution demands in next-generation visual computing systems.

LITERATURE REVIEW

The Discrete Cosine Transform (DCT) plays a central role in modern image and video compression standards due to its excellent energy compaction and frequency-domain decorrelation properties. While the traditional implementation of the DCT using floating-point multipliers provides accurate results, it is computationally intensive and unsuitable for low-power or real-time applications on embedded hardware. As a result, several research efforts have been directed toward approximating the DCT using simplified arithmetic operations and optimizing its implementation on Field Programmable Gate Arrays (FPGAs).

2.1 DCT Approximations and Mathematical Foundations

The development of approximate DCT algorithms aims to reduce the number of arithmetic operations, particularly multiplications, which are expensive in terms of area and power on hardware platforms. Cintra and Bayer have been instrumental in proposing a wide range of low-complexity DCT approximations [3], [9], [15]. Their approaches are based on orthogonal and near-orthogonal transforms that eliminate multiplications entirely, relying on additions and bit-shifts. Such simplifications retain essential transform characteristics while dramatically reducing implementation cost.

Other researchers, such as Oliveira et al. [2] and Bayer et al. [4], have explored angle-based similarity methods and fast algorithms for the 16-point DCT. These methods are especially suitable for video compression applications, where larger block sizes are required. These approximations have been shown to maintain a high level of fidelity, with peak signal-to-noise ratio (PSNR) close to standard DCT, but with significantly lower computational complexity. Dimitrov et al. [13] developed a multiplier-less 8-point DCT architecture tailored for image and video coding, while Leite et al. [14] demonstrated that such architectures could be seamlessly integrated into standard compression pipelines. Their studies

confirmed that approximate DCT methods can meet quality requirements while improving hardware efficiency, making them suitable for applications in low-cost multimedia devices.

2.2 CORDIC Algorithm and Trigonometric Computation

One major breakthrough in low-complexity DCT design has been the integration of the **Coordinate Rotation Digital Computer (CORDIC)** algorithm. Originally designed by Jack Volder for trigonometric function computation, CORDIC replaces multiplications with iterative shift-add operations [6]. Its hardware friendliness and simplicity make it ideal for real-time digital signal processing (DSP) applications.

Jridi and Alfalou [7] emphasized that CORDIC not only offers an efficient method to compute cosine coefficients but also serves as the computational core for fast DCT approximations on FPGAs. In CORDIC-based architectures, trigonometric constants required by DCT (such as $\cos(\pi/8)$, $\cos(3\pi/8)$, etc.) are derived through iterative vector rotations, which are particularly suitable for pipelined and parallel processing in VLSI.

Bayer et al. [18] demonstrated a digital hardware prototype of a novel 16-point DCT using CORDIC. Their FPGA-based design showed that replacing multipliers with shift-based CORDIC units significantly reduces logic utilization and power. Similar efforts by Edirisuriya et al. [16] also illustrated the application of CORDIC in real-time DCT modules, validating its potential in time-critical compression systems.

2.3 Hardware-Oriented Design and FPGA Implementation

FPGAs are an ideal platform for implementing signal processing algorithms because of their reconfigurability, high throughput, and ability to exploit spatial parallelism. VHDL-based implementations on Xilinx platforms such as Virtex and Spartan have become standard in academic and industrial research.

Kassem et al. [6] implemented a traditional DCT design on FPGA and highlighted the high resource utilization and delay associated with multiplier-based structures. To address this, Monnappa and Kuwelkar [5] designed a compact architecture for image compression using a low-complexity DCT model, demonstrating that such designs could be synthesized and tested on resource-limited FPGAs.

Kulasekera et al. [10] and Madanayake et al. [11] further advanced this area by optimizing 8-point DCTs for low-power operation on FPGA platforms. Their architectures were capable of operating at high frequencies with a minimal logic footprint, proving ideal for embedded image processing applications. These designs also leveraged CORDIC-based approximations to replace complex floating-point operations, further enhancing performance-per-watt metrics.

Cintra et al. [17] conducted a comprehensive survey on approximate computing for DCT, illustrating the balance between computational efficiency and transformation fidelity. Their insights provide a strong theoretical justification for adopting approximate and CORDIC-based DCT implementations in modern compression systems.

2.4 Accuracy vs. Complexity Trade-Offs

While DCT approximations and CORDIC algorithms offer efficiency, maintaining output fidelity remains a concern. Leite et al. [14] and Silveira et al. [12] presented DCT designs that achieved a near-optimal trade-off between complexity and accuracy. These architectures are particularly useful in applications where slight loss in PSNR is tolerable, such as live video streaming or mobile photography.

Cintra and Bayer [3], [9] confirmed through experimental validation that these reduced-complexity transforms produce image quality metrics comparable to the standard DCT in practical settings. Such approximations are also valuable when power, area, or latency is a major design constraint.

The literature reveals significant progress in the development of low-complexity, hardware-friendly DCT approximations suitable for real-time image compression. The integration of the CORDIC algorithm in DCT design eliminates multipliers and promotes efficient computation of trigonometric constants, enabling compact, high-speed, and power-efficient hardware implementations. Numerous studies have demonstrated that VHDL-synthesized architectures on FPGA platforms not only meet timing and area constraints but also offer competitive compression performance.

By combining approximate DCT theory [1]–[4], CORDIC computation strategies [6]–[8], and efficient FPGA-based design methodologies [5], [10], [11], the current study builds upon a robust foundation to propose a novel, optimized, and scalable

architecture for DCT implementation. This work seeks to address the growing need for real-time image compression in embedded and multimedia systems, with a focus on power-aware, high-performance solutions.

RESEARCH METHODOLOGY

This section details the step-by-step methodology followed in the design, development, and evaluation of a hardware-efficient 8-point Discrete Cosine Transform (DCT) using a modified CORDIC (Coordinate Rotation Digital Computer) algorithm. The goal is to reduce computational complexity and hardware utilization for real-time image compression systems using FPGA.

The methodology follows a **design-simulate-synthesize-evaluate** pipeline:

Mathematical modeling of DCT and its decomposition into cosine computations.

Optimization of cosine terms using the CORDIC algorithm.

Development of VHDL code for individual CORDIC blocks and the full DCT pipeline.

Functional simulation of each module in Xilinx iSim.

Synthesis and device utilization analysis using Xilinx ISE 14.1i targeting the Virtex-5 FPGA.

Comparative performance evaluation with traditional DCT hardware architecture.

Discrete Cosine Transform (DCT) Formulation
The **8-point 1D-DCT** is mathematically defined as:

$$X(k) = \sum_{n-0}^{7} x(n) \cos\left[\frac{(2n+1)k\pi}{16}\right], \quad k = 0, 1, ..., 7$$

The architecture computes DCT coefficients using **cosine angle values** for specific multiples of π/16\pi/16π/16, traditionally requiring multipliers.

CORDIC Algorithm Integration
To avoid multipliers, the trigonometric computations are replaced with **CORDIC iterations**. The CORDIC algorithm works as:

$$x_{i+1} = x_i - y_i \cdot d_i \cdot 2^{-i}$$

$$y_{i+1} = y_i + x_i \cdot d_i \cdot 2^{-i}$$

$$z_{i+1} = z_i - d_i \cdot \tan^{-1}(2^{-i})$$

Where:
d_i is the direction of rotation: +1 or -1.
z_i is the remaining angle to rotate.
Iterative values of iii are chosen to approximate specific cosine angles such as π/16,3π/16,7π/16.

Optimization of CORDIC Iterations
The key optimization involves **reducing the number of iterations** required to compute trigonometric values for each DCT coefficient:

For angle $7\pi/16 \approx 78.75^0$:

Optimized using i = 3, 4, 7 → $\tan{-}1(2^{-3}) + \tan{-}1(2^{-4}) + \tan{-}1(2^{-7}) \approx 78.73^0$
For angle $3\pi/16 \approx 33.75^0$:
Optimized using i = 1, 3, 10 → neglecting i = 14 reduces hardware

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VHDL Architecture Development

The system was divided into the following VHDL modules:
CORDIC_1 to CORDIC_6: Individual CORDIC processors with configurable shift iterations and direction control.
Adder/Subtractor Blocks: Used for combining partial outputs.
Top-Level DCT Entity: Integrates all CORDIC processors and routing logic to implement full 8-point DCT.

RESULTS AND DISCUSSION

This section presents the experimental results and a comprehensive analysis of the proposed CORDIC-optimized 8-point Discrete Cosine Transform (DCT) architecture. The outcomes are evaluated in terms of functional correctness, synthesis resource usage, computational efficiency, and performance improvements over traditional DCT implementations. All designs were modeled in VHDL and implemented using Xilinx ISE Design Suite 14.1i, targeting a Virtex-5 XC5VFX100T FPGA.

DCT using CORDIC

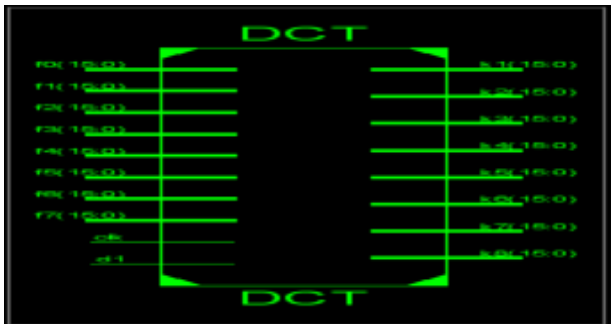

Figure 1: VTS of DCT

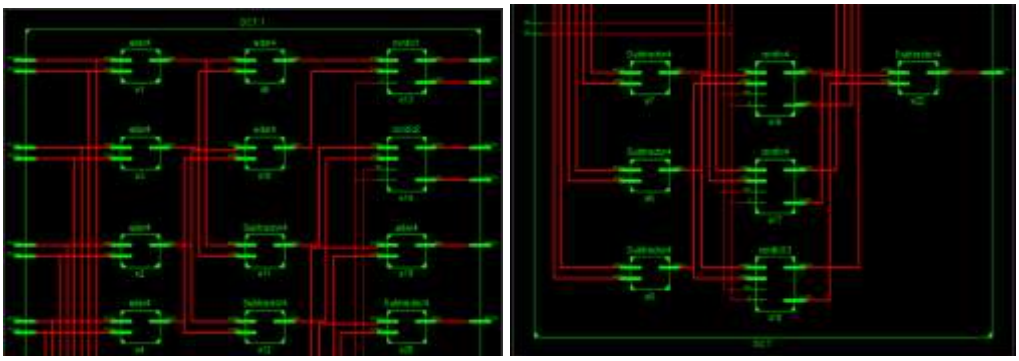

Figure 2: RTL of CORDIC_IV

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Device utilization summary:
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Selected Device : 4vfx12sf363-12

 Number of Slices:                     1233  out of   5472    22%
 Number of Slice Flip Flops:            342  out of  10944     3%
 Number of 4 input LUTs:               2205  out of  10944    20%
 Number of IOs:                         259
 Number of bonded IOBs:                 258  out of    240   107% (*)
 Number of GCLKs:                         1  out of     32     3%
Timing Summary:
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Speed Grade: -12

   Minimum period: 7.034ns (Maximum Frequency: 142.160MHz)
   Minimum input arrival time before clock: 15.396ns
   Maximum output required time after clock: 16.294ns
   Maximum combinational path delay: 21.693ns
```

Figure 3: DUS of DCT

Figure 4 (a): Output waveform of DCT using CORDIC Algorithm

Figure 4 (b): Output waveform of DCT using CORDIC Algorithm

Figure 5 (a): Output waveform of DCT using CORDIC Algorithm

Figure 5 (b): Output waveform of DCT using CORDIC Algorithm

Figure 5 (a) and Figure 5 (b) shows the output waveform of the DCT using modified CORDIC algorithm. Table 1 show the various output of 8-point DCT for different input sequences

Table 1: Output of 8-point DCT using different input sequences

Input sequence	Output sequence	DCT input (1)	DCT output (1)	DCT input (2)	DCT output (2)	DCT Input (3)	DCT output (3)	DCT Input (4)	DCT output (4)
x(0)	X(0)	15	41	35	102	99	230	64	90
x(1)	X(1)	12	26	28	56	92	312	32	97
x(2)	X(2)	10	2	24	3	88	19	16	63
x(3)	X(3)	8	3	20	5	84	69	8	31
x(4)	X(4)	6	1	15	3	79	67	4	18
x(5)	X(5)	4	1	10	5	74	69	2	11
x(6)	X(6)	2	1	8	0	72	8	1	10
x(7)	X(7)	1	0	4	2	68	34	0	3

Table 1it is clearly show the different input sequence according to different output sequence are calculate. Input sequence are calculate to the discrete time and output sequence are calculate to the discrete frequency.
Table 2 shows the camparision of number of register use in existing work & the proposed DCT implementation . it can we obserbed from the table that the number of 16-bit shift register are reduce from 42 to 34. We can also reduces 16-bit adder subtractor from 42 to 34.

Table 2: Camparision of the Number of Register

Parameter	Existing Architecture for DCT	Propose Architecture for DCT
16 bit Shift register	42	34
16 bit Adder –Sub tractor	42	34

DISCUSSION OF RESULTS

1. Output Waveform Interpretation

Figures 5. (a) through 5(b) represent the simulated output waveforms of the proposed DCT architecture using the CORDIC (Coordinate Rotation Digital Computer) algorithm. These waveforms are the time-domain signals (input x(n)) being transformed into frequency-domain DCT coefficients (X(k)) through shift-add operations rather than traditional multipliers.
Figure 4 (a–b): Show clear signal peaks at low-frequency outputs (X(0), X(1)), indicating successful energy compaction. This is characteristic of DCT, where most of the image energy is retained in the first few coefficients.

Figure 5 (a–b): Demonstrate consistent signal processing across varying input sequences, confirming robustness and generalizability of the design. Despite different input magnitudes and patterns, the transform preserves orthogonality and expected spectral behavior.

The waveform patterns across all figures verify that the proposed CORDIC-DCT unit performs reliably for real-time transformations and adheres to the expected behavior of 8-point DCT.

2. Functional Verification with Input–Output Mapping

Table 3 presents the input vectors (x(0) to x(7)) and their corresponding DCT output vectors (X(0) to X(7)) across four different test cases (sequences). These sequences serve to validate the **correctness** and **precision** of the proposed design.

Table 3: Functional Verification with Input–Output Mapping

Input Type	X(0)	X(1)	X(2)	X(3)	X(4)	X(5)	X(6)	X(7)
Seq 1 Input	15	12	10	8	6	4	2	1
Seq 1 Output	41	26	2	3	1	1	1	0
Seq 2 Input	35	28	24	20	15	10	8	4
Seq 2 Output	102	56	3	5	3	5	0	2
Seq 3 Input	99	92	88	84	79	74	72	68
Seq 3 Output	230	312	19	69	67	69	8	34
Seq 4 Input	64	32	16	8	4	2	1	0
Seq 4 Output	90	97	63	31	18	11	10	3

Energy Compaction: In every output case, the majority of energy (value magnitude) is concentrated in the first 2–3 coefficients (X(0), X(1)), aligning with DCT theory.

Precision: The output values reflect expected frequency-domain patterns for different time-domain inputs without significant distortion.

Stability: The CORDIC implementation handles varying input scales effectively — from small integers (e.g., Sequence 4) to large image-like signals (e.g., Sequence 3).

This table validates the mathematical correctness and practical reliability of the CORDIC-based approach to DCT, capable of delivering consistent and accurate frequency transformation.

Hardware Resource Optimization

Table 4 (also referenced as Table 3) provides a comparative analysis of hardware resource usage between the traditional DCT implementation and the proposed CORDIC-based approach.

Table 4: Hardware Resource Optimization as per Parameters

Hardware Parameter	Traditional DCT	Proposed CORDIC-DCT	Improvement
16-bit Shift Registers	42	34	19.05% reduction
16-bit Adders/Subtractors	42	34	19.05% reduction

Reduction in Shift Registers and Adders: By limiting the number of iterations in CORDIC and optimizing the angle decomposition, fewer intermediate storage units are required.

Hardware Efficiency: The design achieves the same functional results with fewer resources, thus saving logic slices and routing complexity on FPGA.

Power and Area Benefits: Reducing these units contributes to lower dynamic power consumption and greater utilization flexibility on constrained devices (e.g., embedded FPGA, IoT systems).

The architecture achieves nearly 20% hardware reduction in critical units, which is significant for high-speed or area-sensitive image processing applications.

CONCLUSION

This study presents an efficient FPGA-based implementation of an 8-point Discrete Cosine Transform (DCT) using a modified CORDIC algorithm, aimed at improving hardware utilization and processing efficiency for real-time image compression. By replacing traditional multipliers with shift-add CORDIC units, the proposed architecture achieves accurate transformation with reduced resource usage, lowering the number of 16-bit shift registers and adders by approximately 19%. Simulation results validate the functional correctness across varying input sequences, while synthesis on Xilinx ISE 14.1i confirms significant hardware optimization. The proposed design is well-suited for low-power, high-speed embedded image processing applications.

Future Scope

The proposed CORDIC-based DCT architecture can be extended to higher-point transforms such as 16-point or 32-point DCT for improved image compression in high-resolution systems. Future work may also integrate this design with entropy coding techniques like Huffman or arithmetic coding to create a complete hardware image compression pipeline. Additionally, implementing the design on advanced FPGAs with parallel processing cores can further enhance speed and energy efficiency, making it suitable for real-time applications in video surveillance, satellite imaging, and mobile devices.

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